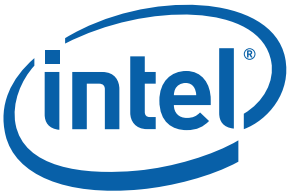

Mobile 5th Generation Intel® Core™ Processor Family I/O, Intel® Core™ M Processor Family I/O, Mobile Intel® Pentium® Processor Family I/O, and Mobile Intel® Celeron® Processor Family I/O

Specification Update

March 2016

Revision 004

Document #: 330838-004

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Contents

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Revision History

Revision	Description	Date
001	• Initial Release	September 2014
002	• Added U-Processor — Mobile 5th Generation Intel® Core™ Processor Family I/O — Mobile Intel® Pentium® Processor Family I/O — Mobile Intel® Celeron® Processor Family I/O • Errata — Added Errata 21-22	January 2015
003	• Errata — Modified erratum 16	March 2015
004	• Errata — Added Errata 23-24	March 2016

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Preface

This document is an update to the specifications contained in the Affected Documents table below. This document is a compilation of device and documentation errata and specification changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents

Title	Document Number
Mobile 5th Generation Intel® Core™ Processor Family I/O, Intel® Core™ M Processor Family I/O, Mobile Intel® Pentium® Processor Family I/O, and Mobile Intel® Celeron® Processor Family I/O Datasheet	330837

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

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Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the product. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Stepping

X:	Erratum exists in the stepping indicated. Specification Change that applies to the stepping indicated.
(No mark) or (Blank box):	This erratum is fixed or not applicable in listed stepping or Specification Change does not apply to listed stepping.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Erratum Number	Stepping	Status	ERRATA
	B2		
1	X	No Fix	USB Isoch In Transfer Error Issue
2	X	No Fix	USB Babble Detected with SW Overscheduling
3	X	No Fix	USB Full-/low-speed EOP Issue
4	X	No Fix	Asynchronous Retries Prioritized Over Periodic Transfers
5	X	No Fix	USB FS/LS Incorrect Number of Retries
6	X	No Fix	USB Full-/Low-speed Port Reset or Clear TT Buffer Request
7	X	No Fix	xHC Data Packet Header and Payload Mismatch Error Condition
8	X	No Fix	USB SuperSpeed Packet with Invalid Type Field Issue
9	X	No Fix	xHC Behavior with Three Consecutive Failed U3 Entry Attempts
10	X	No Fix	Incorrect IRQ(x) Vector Returned for 8259 Interrupts With RAEOI Enabled
11	X	No Fix	USB RMH Think Time Issue
12	X	No Fix	Max Packet Size and Transfer Descriptor Length Mismatch
13	X	No Fix	USB Full-/low-speed Device Removal Issue
14	X	No Fix	PCIe Root Ports Unsupported Request Completion
15	X	No Fix	SATA Signal Voltage Level Violation
16	X	No Fix	SMBus Hold Time
17	X	No Fix	RMH Port Disabled Due to Device Initiated Remote Wake
18	X	No Fix	Enumeration Issue when Resuming for Sx
19	X	No Fix	USB xHCI may Execute a Stale Transfer Request Block (TRB)
20	X	No Fix	xHCI Controller OC# Issue
21	X	No Fix	xHCI USB2.0 Split-Transactions Error Counter Reset Issue
22	X	No Fix	Intel® Smart Sound Technology DSP Initialization Issue
23	X	No Fix	xHCI Host Controller Reset May Cause a System Hang
24	X	No Fix	PCI Express Gen2 x4 Device may cause a Machine Check Exception

Specification Changes

Number	Stepping	SPECIFICATION CHANGES
	B2	
	X	There are no Specification Changes in this revision of the specification update.

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Errata

1. USB Isoch In Transfer Error Issue

Problem: If a USB full-speed inbound isochronous transaction with a packet length 190 bytes or greater is started near the end of a microframe the PCH may see more than 189 bytes in the next microframe.

Implication: If the PCH sees more than 189 bytes for a microframe an error will be sent to software and the isochronous transfer will be lost. If a single data packet is lost no perceptible impact for the end user is expected.

Note: Intel has only observed the issue in a synthetic test environment where precise control of packet scheduling is available, and has not observed this failure in its compatibility validation testing.

- Isochronous traffic is periodic and cannot be retried thus it is considered good practice for software to schedule isochronous transactions to start at the beginning of a microframe. Known software solutions follow this practice.
- To sensitize the system to the issue additional traffic such as other isochronous transactions or retries of asynchronous transactions would be required to push the inbound isochronous transaction to the end of the microframe.

Note: When all USB ports are routed to the xHCI, this RMH erratum will have no impact.

Workaround: None.

Status: No Plan to Fix

2. USB Babble Detected with SW Overscheduling

Problem: If software violates USB periodic scheduling rules for full-speed isochronous traffic by overscheduling, the RMH may not handle the error condition properly and return a completion split with more data than the length expected.

Implication: If the RMH returns more data than expected, the endpoint will detect packet babble for that transaction and the packet will be dropped. Since overscheduling occurred to create the error condition, the packet would be dropped regardless of RMH behavior. If a single isochronous data packet is lost, no perceptible impact to the end user is expected.

Note: USB software overscheduling occurs when the amount of data scheduled for a microframe exceeds the maximum budget. This is an error condition that violates the USB periodic scheduling rule.

Note: This failure has only been recreated synthetically with USB software intentionally overscheduling traffic to hit the error condition.

Note: When all USB ports are routed to the xHCI, this RMH erratum will have no impact.

Workaround: None.

Status: No Plan to Fix

3. USB Full-/low-speed EOP Issue

Problem: If the EOP of the last packet in a USB Isochronous split transaction (Transaction >189 bytes) is dropped or delayed 3 ms or longer the following may occur:

- If there are no other pending low-speed or full-speed transactions the RMH will not send SOF, or Keep-Alive. Devices connected to the RMH will interpret this condition as idle and will enter suspend.
- If there is other pending low-speed or full-speed transactions, the RMH will drop the isochronous transaction and resume normal operation.

Implication:

- If there are no other transactions pending, the RMH is unaware a device entered suspend and may starting sending a transaction without waking the device. The implication is device dependent, but a device may stall and require a reset to resume functionality.
- If there are other transactions present, only the initial isochronous transaction may be lost. The loss of a single isochronous transaction may not result in end user perceptible impact.

Note: Intel has only observed this failure when using software that does not comply with the USB specification and violates the hardware isochronous scheduling threshold by terminating transactions that are already in progress

Note: When all USB ports are routed to the xHCI, this RMH erratum will have no impact.

Workaround: None.

Status: No Plan to Fix

4. Asynchronous Retries Prioritized Over Periodic Transfers

Problem: The integrated USB RMH incorrectly prioritizes full-speed and low-speed asynchronous retries over dispatchable periodic transfers.

Implication: Periodic transfers may be delayed or aborted. If the asynchronous retry latency causes the periodic transfer to be aborted, the impact varies depending on the nature of periodic transfer:

- If a periodic interrupt transfer is aborted, the data may be recovered by the next instance of the interrupt or the data could be dropped.
- If a periodic isochronous transfer is aborted, the data will be dropped. A single dropped periodic transaction should not be noticeable by end user.

Note: This issue has only been seen in a synthetic environment. The USB spec does not consider the occasional loss of periodic traffic a violation.

Note: When all USB ports are routed to the xHCI, this RMH erratum will have no impact.

Workaround: None.

Status: No Plan to Fix

5. USB FS/LS Incorrect Number of Retries

Problem: A USB low-speed transaction may be retried more than three times, and a USB full-speed transaction may be retried less than three times if all of the following conditions are met:

- A USB low-speed transaction with errors, or the first retry of the transaction occurs near the end of a microframe, and there is not enough time to complete another retry of the low-speed transaction in the same microframe.
- There is pending USB full-speed traffic and there is enough time left in the microframe to complete one or more attempts of the full-speed transaction.
- Both the low-speed and full-speed transactions must be asynchronous (Bulk/Control) and must have the same direction either in or out.

Note: Per the USB EHCI Specification a transaction with errors should be attempted a maximum of 3 times if it continues to fail.

Note: When all USB ports are routed to the xHCI, this RMH erratum will have no impact.

Implication:

- For low-speed transactions the extra retry(s) allow a transaction additional chance(s) to recover regardless of if the full-speed transaction has errors or not.
- If the full-speed transactions also have errors, the PCH may retry the transaction fewer times than required, stalling the device prematurely. Once stalled, the implication is software dependent, but the device may be reset by software.

Workaround: None

Status: No Plan to Fix

6. USB Full-/Low-speed Port Reset or Clear TT Buffer Request

Problem: One or more full-/low-speed USB devices on the same RMH controller may be affected if the devices are not suspended and either (a) software issues a Port Reset OR (b) software issues a Clear TT Buffer request to a port executing a split full-/low-speed Asynchronous Out command.

- The small window of exposure for full-speed device is around 1.5 microseconds and around 12 microseconds for a low-speed device.

Implication: The affected port may stall or receive stale data for a newly arrived split transfer occurring at the time of the Port Reset or Clear TT Buffer request.

Note: This issue has only been observed in a synthetic test environment.

Note: When all USB ports are routed to the xHCI, this RMH erratum will have no impact.

Workaround: None.

Status: No Plan to Fix

7. xHC Data Packet Header and Payload Mismatch Error Condition

Problem: If a SuperSpeed device sends a DPH (Data Packet Header) to the xHC with a data length field that specifies less data than is actually sent in the DPP (Data Packet Payload), the xHC will accept the packet instead of discarding the packet as invalid.

Note: The USB 3.0 specification requires a device to send a DPP matching the amount of data specified by the DPH.

Implication: The amount of data specified in the DPH will be accepted by the xHC and the remaining data will be discarded and may result in anomalous system behavior.

Note: This issue has only been observed in a synthetic test environment with a synthetic device.

Workaround: None.

Status: No Plan to Fix

8. USB SuperSpeed Packet with Invalid Type Field Issue

Problem: If the encoding for the "type" field for a SuperSpeed packet is set to a reserved value and the encoding for the "subtype" field is set to "ACK", the xHC may accept the packet as a valid acknowledgement transaction packet instead of ignoring the packet.

Note: The USB 3.0 specification requires that a device never set any defined fields to reserved values.

Implication: System implication is dependent on the misbehaving device and may result in anomalous system behavior.

Note: This issue has only been observed in a synthetic test environment with a synthetic device.

Workaround: None.

Status: No Plan to Fix

9. xHC Behavior with Three Consecutive Failed U3 Entry Attempts

Problem: The xHC does not transition to the SS.Inactive USB 3.0 LTSSM (Link Training and Status State Machine) state after a SuperSpeed device fails to enter U3 upon three consecutive attempts.

Note: The USB 3.0 specification requires a SuperSpeed device to enter U3 when directed.

Implication: The xHC will continue to try to initiate U3. The implication is driver and operating system dependent.

Workaround: None.

Status: No Plan to Fix

10. Incorrect IRQ(x) Vector Returned for 8259 Interrupts With RAEOI Enabled

Problem: If multiple interrupts are active prior to an interrupt acknowledge cycle with Rotating Automatic End of Interrupt (RAEOI) mode of operation enabled for 8259 interrupts (0-7), an incorrect IRQ(x) vector may be returned to the processor.

Implication: Implications of an incorrect IRQ(x) vector being returned to the CPU are SW implementation dependent.

Note: This issue has only been observed in a synthetic test environment.

Workaround: None.

Status: No Plan to Fix

11. USB RMH Think Time Issue

Problem: The USB RMH Think Time may exceed its declared value in the RMH hub descriptor register of 8 full-speed bit times.

Implication: If the USB driver fully subscribes a USB microframe, LS/FS transactions may exceed the microframe boundary.

Note: No functional failures have been observed.

Note: When all USB ports are routed to the xHCI, this RMH erratum will have no impact.

Workaround: None.

Status: No Plan to Fix

12. Max Packet Size and Transfer Descriptor Length Mismatch

Problem: The xHC may incorrectly handle a request from a low-speed or full-speed device when all the following conditions are true:

- The sum of the packet fragments equals the length specified by the TD (Transfer Descriptor)
- The TD length is less than the MPS (Max Packet Size) for the device
- The last packet received in the transfer is “0” or babble bytes

Implication: The xHC will halt the endpoint if all the above conditions are met. All functions associated with the endpoint will stop functioning until the device is unplugged and reinserted.

Workaround: None.

Status: No Plan to Fix

13. USB Full-/low-speed Device Removal Issue

Problem: If two or more USB full-/low-speed devices are connected to the same USB controller, the devices are not suspended, and one device is removed, one or more of the devices remaining in the system may be affected by the disconnect.

Implication: The implication is device dependent. A device may experience a delayed transaction, stall and be recovered via software, or stall and require a reset such as a hot plug to resume normal functionality.

Note: When all USB ports are routed to the xHCI, this RMH erratum will have no impact.

Workaround: None.

Status: No Plan to Fix

14. PCIe Root Ports Unsupported Request Completion

Problem: The PCIe* root ports may return an Unsupported Request (UR) completion with an incorrect lower address field in response to a memory read if any of the following occur:

- Bus Master Enable is disabled in the PCIe Root Port's Command register (PCICMD bit 2 =0)
- Address Type (AT) field of the Transaction Layer Packet (TLP) header is non-zero
- The requested upstream address falls within the memory range claimed by the secondary side of the bridge
- Requester ID with Bus Number of 0

Implication: The UR Completion with an incorrect lower address field may be handled as a Malformed TLP causing the Requestor to send an ERR_NONFATAL or ERR_FATAL message upstream to the root port.

Workaround: None.

Status: No Plan to Fix

15. SATA Signal Voltage Level Violation

Problem: SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, the SATA transmit signaling voltage levels may exceed the maximum motherboard TX connector and device RX connector voltage specifications as defined in section 7.2.2.3 of the Serial ATA specification, rev 3.1. This issue applies to Gen 1 (1.5 Gb/s).

Implication: None known.

Workaround: None.

Status: No Plan to Fix

16. SMBus Hold Time

Problem: The SMBus data hold time may be less than the 300 ns minimum defined by the Platform Controller Hub Datasheet.

Implication: There are no known functional failures due to this issue.

Workaround: None.

Status: No Plan to Fix

17. RMH Port Disabled Due to Device Initiated Remote Wake

Problem: During resume from Global Suspend, the RMH controller may not send SOF soon enough to prevent a device from entering suspend again. A collision on the port may occur if a device initiated remote wake occurs before the RMH controller sends SOF.

Note: Intel has only observed this issue when two USB devices on the same RMH controller send remote wake within 30 ms window while RMH controller is resuming from Global Suspend

Note: When all USB ports are routed to the xHCI, this RMH erratum will have no impact.

Implication: The RMH host controller may detect the collision as babble and disable the port.

Workaround: Intel recommends system software to check bit 3 (Port Enable/Disable Change) together with bit 7 (Suspend) of Port N Status and Control PORTC registers when determining which port(s) have initiated remote wake.

Status: No Plan to Fix

18. Enumeration Issue when Resuming for Sx

Problem: If a device is attached while the platform is in S3 or S4 and the device is assigned the highest assignable Slot ID upon resume, the xHC may attempt to access an unassigned main memory address.

Implication: Accessing unassigned main memory address may cause a system software timeout leading to possible system hang.

Workaround: System Software can detect the timeout and perform a host controller reset to avoid the system hang.

Note: Microsoft* Windows 8* xHC in-box driver detects and performs a host controller reset. The Intel Windows 7* xHC driver revision 2.5.0.19 or later will also detect and perform the host controller reset.

Status: No Plan to Fix

19. USB xHCI may Execute a Stale Transfer Request Block (TRB)

Problem: When a USB 3.0 or USB 2.0 hub with numerous active Full-Speed (FS) or Low-Speed (LS) periodic endpoints attached is removed and then reconnected to an USB xHCI port, the xHCI controller may fail to fully refresh its cache of TRB records. The controller may read and execute a stale TRB and place a pointer to it in a Transfer Event TRB.

Implication: In some cases, the xHCI controller may read de-allocated memory pointed to by a TRB of a disabled slot. The xHCI controller may also place a pointer to that memory in the event ring, causing the xHCI driver to access that memory and process its contents, resulting in system hang, failure to enumerate devices, or other anomalous system behavior.

Note: This issue has only been observed in a stress test environment.

Workaround: None.

Note: A BIOS code change to reduce the occurrence of this erratum has been identified and implemented in the latest BIOS reference code.

Status: No plan to fix.

20. xHCI Controller OC# Issue

Problem: xHCI Host Controller Reset (HCRST) may not complete if a USB over-current event occurs while powering on or resuming from S5 or S4.

Implication: Upon resume all xHCI Ports may become non-functional.

NOTE: To recover xHCI port funtionality requires the USB Device causing an overcurrent event to be removed and the system to be reset.

Workaround: None.

Status: No plan to fix.

21. xHCI USB2.0 Split-Transactions Error Counter Reset Issue

Problem: The xHCI controller may not reset its split transaction error counter if a high-speed USB hub propagates a mal-formed bit from a low-speed or full-speed USB device exhibiting non-USB specification compliant signal quality.

Implication: The implication is device dependent.

- Full Speed and Low Speed devices behind the hub may be re-enumerated and may cause a device to not function as expected.

Workaround: None.

Status: No plan to fix.

22. Intel® Smart Sound Technology DSP Initialization Issue

Problem: On BDW U/Y designs implementing Intel Smart Sound Technology (SST) when resuming from idle audio condition where the DSP is placed in D3 power state and power gated, the DSP may not be initialized properly.

Implication: Loss of audio input and output functionality may occur. Audio applications may indicate an issue with audio functionality. No system hangs observed during failure.

Workaround: A BIOS and Intel SST driver change has been identified and may be implemented as a workaround for this erratum.

Status: No plan to fix.

23. xHCI Host Controller Reset May Cause a System Hang

Problem: xHCI Host Controller may not respond following system software setting (Bit 1 = '1') the Host Controller Reset (HCRST) of the USB Command Register (xHCIBAR + 80h).

Implication: CATERR may occur resulting in a system hang.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix

24. PCI Express Gen2 x4 Device may cause a Machine Check Exception

Problem: PCH PCI Express Host Controller when configured as Gen2 x4 may not properly handle an abrupt link transition to electrical idle without receiving Electrical Idle Ordered Set (EIOS) such as during hot unplug event.

Implication: Platform May Hang due to a Machine Check Exception if all of the following conditions are met when the link is terminated abruptly:

- No 8b10b errors occur,
- A TLP of exactly 3DWords is received (length started to count from STP as the first byte)
  Note: A valid TLP length is 5DWords at least),
- The TLP must end with END or EDB,
- And dependent on the specific internal timing of the DW alignment.

Workaround: None

Status: No Fix

Specification Changes

No Specification Changes in this revision of the Specification Update.

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